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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,896	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10-12,14-17,20-22,24-30 and 33-53* is/are rejected.

7)☒ Claim(s) *3,9,13,18,19,23,31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/26/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

This Office Action is responsive to the application filed on 26 November 2003. Acknowledgment is made of applicant's claim for domestic priority under 35 U.S.C. 120. Claims 1-53 are presented for examination.

Claims 1-53 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 26 November 2003 was filed after the mailing date of the application on 26 November 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir.

1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 4-7, 10, 11, 14-16, 21, 24, 26, 28, 29, 34, 36, 38-40, 45, 49, 50, and 52 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 4, 9, 10, 12, 13, 15, 20, 21, 24, 30, 31, 33, 34, 41, 42, 43, 46 and 49 of co-pending Application No.10724472. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claimed invention in the present application is an obvious derivation from the co-pending application, as both of the instant invention and the co-pending applications describe reading, shifting, and storing a cache line in a cache memory using barrel shifter, wherein the cache memory is associated with a main memory comprising a DRAM and the cache comprising a Level 1 cache.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 12, 35, and 45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claims 2, 12, and 35, it is unclear to the Examiner if the "entire cache line" is one of the cache lines of the data cache in the claims, or from another data source. The Examiner is rejecting the claims in light of the first interpretation. Appropriate correction is required.

As for claim 45, it is unclear to the Examiner which is cache line in the "plurality of cache lines" is referred by "the cache line". The Examiner is rejecting the claims by interpreting the "the cache line" as any one of the "plurality of cache lines". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21, 30, 33, 34, 41, 42, 45, 51 and 53 are rejected under 35 U.S.C 102(b) as being unpatentable over Groves [5,222,225] (hereinafter "Groves").

As for claims 21, 34 and 45, Groves teaches a processor (Fig 1) for data string manipulation comprising:

a data cache means (Fig 1, 20 Memory; Col 3, Line 68; Col 4, Line 1) for storing a plurality of cache lines comprising a plurality of bytes of data (Fig 2A);

a string execution means for manipulating the data in the data cache means, the string execution means coupled to said data cache means (Fig 1, 30 Byte Merge, 22 Byte Rotator); and

a means for shifting the cache line (Fig 1, 22 Byte Rotator) coupled to the data cache so as to shift a cache line a selected number of bytes (Col 6, Lines 3-30).

It is also clear the method of claim 21 is performed by the processors of claims 34 and 45.

As for claims 30, 41 and 51, Groves further teaches a bus interface unit (Fig 2B, 18A Memory Bus suggests the existence of a bus interface) is coupled to the string execution unit (Fig 2B, 18A Memory Bus and 22A Byte Rotate; Col 6, Lines 5-9).

As for claims 33, 42 and 53, Groves further teaches coupling a register to the cache line shifter so as to store data shifted out of the cache line by the cache line shifter (Col 6, Lines 3-42; Col 6, Lines 12-30; a rotator stores data shifted out of one end back to the other end).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 7, 8, 11, 17, 20, 24, 25, 36, 37 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Groves, further in view of Pogue [4,920,483] (hereinafter "Pogue").

As for claims 1, 11, 24, 25, 36, 37 and 52, Groves already substantially discloses the claims as described above, but does not particularly point out that the shifter is a barrel shifter which shifts an entire cache line a selected number of bytes in a single processor cycle. However, Pogue teaches a memory system which includes a barrel shifter that shifts a plurality of bits in a single processor cycle, in order to save the number of cycles used for the shift operation. Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that a barrel shifter can be used in Groves' cache memory to facilitate shifting of the entire cache line in order to save processing time.

As for claims 7 and 20, Groves further teaches coupling a register to the barrel shifter so as to store data shifted out of the cache line by the barrel shifter (Col 6, Lines 3-42; Col 6, Lines 12-30; a rotator stores data shifted out of one end back to the other end).

As for claims 8 and 17, Groves further teaches a bus interface unit (Fig 2B, 18A Memory Bus suggests the existence of a bus interface) is coupled to the barrel shifter (Fig 2B, 18A Memory Bus and 22A Byte Rotate; Col 6, Lines 5-9).

Claims 2, 12, 22, 35, 43, 44, 46, 47, 48 are rejected under 35 U.S.C 103(a) as being unpatentable over Groves and Pogue, in further view of Lee [5,060,143] (hereinafter "Lee").

As for claims 2, 12, 22, 35, 46 and 47, Groves in combination with Pogue already substantially discloses the claims as described above, but does not particularly point out a plurality of comparators coupled to the data cache so as to compare data in an entire cache line to a test data string in a single processor cycle. However, Lee teaches a data string manipulation processor that includes a plurality of comparators to compare an group of bytes in a data array to a test data string in a single processor cycle (Fig 3, 140 Comparator Array; Col 1, Lines 53-56; a comparison operation determines the propagation delay of a pipeline stage, which in turn determines the length of a clock cycle in a pipelined processor). It would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Lee's comparators can be included in Groves' cache memory system in order to reduce the processing time of the compare operation.

As for claims 43 and 44, Groves and Pogue already substantially disclose the claim as described above in further view of Lee, and Lee further teaches a decoder coupled to the plurality of comparators so as to identify a portion of the cache line that contains data matching at least a portion of the test data string (Col 8, Lines 1-4; Col 8; Lines 44-54), wherein the decoder is coupled to the string execution unit and is

configured to forward a cache address of the matching cache line data to the string execution unit (Col 8, Lines 1-4). It would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that this feature is useful in Grove's cache memory to identify the location of the matching data.

As for claim 48, Groves and Pogue, in further view of Lee, already substantially disclose the claim as described above, and further teach that the number of the plurality of comparators is equal to the number of bytes in the cache line (Lee: Col 4, Lines 8-11, 4 bytes and 4 comparators; Groves: Fig 2A, one cache line in Memory/Cache is 4 bytes) in order to compare the entire cache line to the data value in one clock cycle (Lee: Col 1, Lines 53-56; a comparison operation determines the propagation delay of a pipeline stage, which in turn determines the length of a clock cycle in a pipelined processor). It would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that this feature can be added to Grove's cache memory to enable comparison of the entire cache line in one clock cycle.

Claims 4, 5, 6, 14, 15, 16, 28, 29, 39, 40, 49 and 50 are rejected under 35 U.S.C 103(a) as being unpatentable over Groves and Pogue, in further view of Tran [5,900,012] (hereinafter "Tran").

As for claims 4, 5, 6, 14, 15, 16, 28, 29, 39, 40, 49 and 50, Groves already substantially discloses the claims in further view of Pogue, but does not specifically point out the string execution unit is in association with a memory controller, which is coupled to a main memory that comprises a DRAM circuit. However, Tran teaches a cache system where a cache line is moved from its original location in the cache to first destination cache line (Col 6, Lines 26-39), and the cache data has an associated main memory which comprises a DRAM circuit (Col 1, Liens 36-39), which uses cheaper technology to manufacture than cache memory, and an associated memory controller (a cache memory and main memory require a memory controller), for larger storage capacity (Col 1, Lines 36-39). Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Groves cache memory system could have an associated main memory comprising a DRAM circuit for larger storage capacity than the cache memory at a lower cost.

Claims 10, 26, 38 are rejected under 35 U.S.C 103(a) as being unpatentable over Groves and Pogue, in further view of Papworth et al. [5,404,473] (hereinafter "Papworth").

As for claims 10, 26 and 38, Groves already substantially discloses the claim as described above, but does not particularly point that the data cache comprises a Level 1 cache. However, Papworth teaches discloses a processing system that handles string

operations which comprises a Level 1 cache, in order to improve processing speed (Col 6, Lines 5-8). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Groves' cache memory can incorporate a Level 1 cache in order to improve processing speed

Claim 27 is rejected under 35 U.S.C 103(a) as being unpatentable over Groves, in further view of Papworth.

As for claim 27, Groves already substantially discloses the claim as described above, but does not particularly point that the data cache comprises a Level 2 cache. However, Papworth discloses a processing system that handles string operations which comprises a Level 2 cache, in order to increase storage capacity (Col 6, Lines 5-8). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Groves' cache memory can incorporate a Level 2 cache in order to improve storage capacity.

Allowable Subject Matter

Claims 3, 9, 13, 18, 19, 23, 31, and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Assistant Examiner
Art Unit 2189

5 December 2005

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER